Two-Stage CMOS Operational Amplifier Design with SKY130

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1. Introduction

The operational amplifier (often called "op-amp") is device that amplifies a differential input into a single-ended output voltage. This project and report will focus on the voltage-feedback op-amp, which amplifies the voltage difference between the inputs.

The output voltage of the op-amp can be given by

$$V_{\text{out}} = A_v \left(V_+ - V_-\right), \tag{1.1}$$

where V_+ is the non-inverting input, V_- is the inverting input, and A_v is the open-loop gain of the op-amp. An ideal op-amp will have many characteristics, such as infinite open-loop gain A_v, infinite input resistance R_{in}, zero output resistance R_{out}, infinite bandwidth, zero phase shift, and infinite slew rate. Of course, these cannot be physically realised and are limited by real world constraints among other limitations. Operational amplifier designs must therefore carefully balance their characteristics and make trade-offs to achieve their desired performance metrics.

In this project, we will design and simulate a two-stage complementary MOSFET (CMOS) operational amplifier, implemented in SkyWater's SKY130 open source 130 nm process development kit (PDK).[1] This report will first outline the topology used and design objectives, then go over the design process using open source software tools, and finally an analysis of performance results.

1.1. Design Objectives

Parameter	Symbol	Specification
Supply voltage	V_{DD}	1.8 V
Reference voltage	V_{SS}	0 V
Input common-mode voltage	$V_{\text{in(CM)}}$	0.9 V
Output common-mode voltage	$V_{\text{out(CM)}}$	0.9 V
Power consumption	P	$\leq$ 0.4 mW
Differential output swing	ΔV_{out}	$\geq$ 1.2 V
Low-frequency differential gain	A_{v}	$\geq$ 46 dB
Small-signal unity gain frequency	f_{u}	$\geq$ 60 MHz
Phase margin	ϕ_{m}	$\geq$ 60° & $\leq$ 90°
Slew rate	S	$\geq$ 20 V/µs

Table 1.1. Project design objectives.

1.2. Physical Constraints

Parameter	Symbol	Constraint
Maximum length of transistor	L_{max}	650 nm
Maximum width per multiplier	W_{max}	4 µm
Maximum fingers per multiplier	$N_{\text{f, max}}$	1
Maximum number of multipliers	M_{max}	50

Table 1.2. Physical design constraints.

2. Circuit Design

2.1. Design Topology

We will employ a two-stage amplifier design. The first stage is a high-gain differential-to-differential amplifier, and the second stage is a high-swing differential-to-single-ended amplifer. Since we have a differential voltage in between

[1] https://github.com/google/skywater-pdk.

the two stages, a common-mode feedback circuit is also needed to regulate the DC voltage.

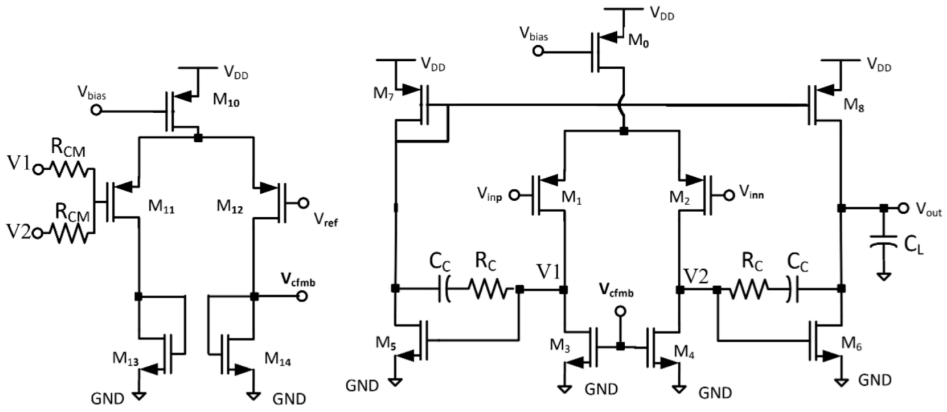

Figure 2.1. Design topology of the operational amplifier.

3. Simulation Results

3.1. Performance Overview

Parameter	Symbol	Specification	Achieved
Supply voltage	V_{DD}	1.8 V	1.8 V
Reference voltage	V_{SS}	0 V	0 V
Input common-mode voltage	$V_{\mathrm{in(CM)}}$	0.9 V	0.9 V
Output common-mode voltage	$V_{\mathrm{out(CM)}}$	0.9 V	0.898 V
Power consumption	P	$\leq$ 0.4 mW	282.2 µW
Differential output swing	ΔV_{out}	$\geq$ 1.2 V	?
Low-frequency differential gain	A_{v}	$\geq$ 46 dB	50.48 dB
Small-signal unity gain frequency	f_{u}	$\geq$ 60 MHz	66.2 MHz
Phase margin	ϕ_{m}	$\geq$ 60° & $\leq$ 90°	75.2°
Slew rate	S	$\geq$ 20 V/µs	75.8 V/µs

Table 3.1. Performance results of the final design.

4. Conclusion